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EXAMINER	
HE, AMY	

ART UNIT	PAPER NUMBER
2831	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,519	BENEDIKT ET AL.	
	Examiner	Art Unit	
	AMY HE	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30* is/are allowed.

6)☒ Claim(s) *1-8, 10, 12-24, 27-29 and 31-33* is/are rejected.

7)☒ Claim(s) *9,11,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Claims 1-7 and 10-33 in the reply filed on March 26, 2009 is acknowledged. Applicant's traversal is persuasive and accordingly, the Restriction Requirement dated February 26, 2009 has been withdrawn.

Claim Objections

2. Claims 8 and 25 are objected to because of the following informalities:

1) In Claim 8, delete "any preceding" before "claim 1" (on line 1).

2) In Claim 25, replace "claim 16" (on line 2) with --claim 1--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7, 10, 12-22, 27 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Ferrero (U. S. Patent No. 6, 509,743).

As for claim 1, Ferrero discloses (right-hand side of Fig. 4 ; Fig. 6; claim 1) an analyser for measuring at frequencies within a frequency range (500MHz to 110GHz,

see claim 1) the response of an electronic device (E) to a high frequency input signal, the analyser including:

an active load pull circuit connectable in use to a device to be analyzed, the active load pull circuit including a feedback circuit (see the feedback circuit as shown in Fig. 4 and 6) arranged (i) to receive an output signal from the device to be analyzed (E), (ii) to modify the signal (using the band filter Rf, amplifier Am, and phase and magnitude control system represented by variable attenuator Ra and a variable phase shifter Rs) and (iii) to feed the modified signal back to the device to be analyzed(E), wherein the feedback circuit is arranged to limit the magnitude gain of the feedback circuit at all frequencies within the frequency range (col. 5, lines 12-55; right-hand side of Fig. 4; Fig. 6).

As for claim 14, Ferrero discloses an active load pull circuit for use in an analyser for measuring at frequencies within a frequency range (500MHz to 110GHz, see claim 1) the response of an electronic device (E) to a high frequency input signal, the active load pull circuit being connectable in use to a device to be analyzed (E) and including a feedback circuit (see the feedback loop in right-hand side of Fig. 4 and Fig. 6) arranged to receive an output signal from the device to be analyzed(E), to modify the signal (using the band filter Rf, amplifier Am, and phase and magnitude control system represented by variable attenuator Ra and a variable phase shifter Rs) and to feed the modified signal back to the device to be analyzed(E), wherein the feedback circuit is arranged to limit the magnitude gain of the feedback circuit at all frequencies within the frequency range(col. 5, lines 12-55; right-hand side of Fig. 4; Fig. 6).

As for claim 16, Ferrero discloses a method of measuring the response of an electronic device (E) to a high frequency input signal, the method including the steps of: providing an electronic device to be analyzed (E), applying a high frequency signal to the device, and modifying (using the band filter Rf, amplifier Am, and phase and magnitude control system represented by variable attenuator Ra and a variable phase shifter Rs) an output signal from the device and then feeding the modified signal back to the device, thereby forming a feedback loop (see the feedback loop as shown in the right-hand side of Fig. 4 and Fig. 6), and measuring (by using the measurement device Sm), at a plurality of frequencies within a frequency range(500MHz to 110GHz, see claim 1), the response of the device to the signal applied to the device, wherein the magnitude gain of the feedback loop is limited at frequencies within the frequency range(col. 5, lines 12-55; right-hand side of Fig. 4; Fig. 6).

As for claims 2, 3 and 15, Ferrero discloses the analyser according to claim 1, wherein the-analyser is so arranged that the magnitude gain and the phase change of the feedback circuit at one or more frequencies within the frequency range is able to be adjusted (using the phase and magnitude control system represented by variable attenuator Ra and a variable phase shifter Rs , as shown in right-hand side of Fig. 4).

As for claim 4, Ferrero discloses the analyser according to claim 1, wherein the feedback circuit is arranged to restrict the phase change (using the phase shifter Rs) effected by the feedback circuit at all frequencies within the frequency range.

As for claims 5 and 7, Ferrero discloses a band filter (band filter Rf) having a bandwidth, covering frequencies within the range, or of greater than 10MHz (500MHz to 110GHz, see claim 1).

As for claim 6, Ferrero discloses a high frequency band filter circuit (band filter Rf) arranged to filter signals in or from the feedback circuit before they are fed back to the device, the band filter circuit having a bandwidth covering frequencies within the range.

As for claim 10, Ferrero discloses a signal processor able in use to modify (using the band filter Rf, amplifier Am, and phase and magnitude control system represented by variable attenuator Ra and a variable phase shifter Rs) the signal from the device to be analyzed by a preselectable amount.

As for claim 12, Ferrero discloses a signal generator (the means for generating the test signal, such as the signal source in Fig. 1) arranged to send an input signal to the device to be analyzed (E).

As for claim 13, Ferrero discloses a signal measuring device (Sm) for measuring loads arising in response to the signals applied to the device to be analyzed.

As for claim 17, Ferrero discloses that the phase change effected by the feedback loop is restricted at frequencies within the frequency range (by using the variable phase shifter Rs).

As for claims 18-20, Ferrero discloses a step of preselecting the way in which the output signal from the device is modified; or preselecting a magnitude gain applied to the output signal from the device; or preselecting a phase change applied to the output

signal from the device (i.e., by preselecting the phase shifter or variable attenuator to be used in the feedback circuit design).

As for claim 21, Ferrero discloses that the step of modifying the output signal from the device includes filtering (using band filter Rf) out signals having frequencies outside a band of frequencies covering frequencies within the frequency range.

As for claim 22, Ferrero discloses that the fundamental frequency of the signal applied to the device can be over 1 GHz (see claim 1).

As for claim 27, Ferrero discloses a method according to claim 16, wherein the method is performed with an analyzer, the analyser including:

an active load pull circuit connectable in use to a device to be analyzed, the active load pull circuit including a feedback circuit (see the feedback circuit as shown in Fig. 4 and 6) arranged (i) to receive an output signal from the device to be analyzed (E), (ii) to modify the signal (using the band filter Rf, amplifier Am, and phase and magnitude control system represented by variable attenuator Ra and a variable phase shifter Rs) and (iii) to feed the modified signal back to the device to be analyzed(E), wherein the feedback circuit is arranged to limit the magnitude gain of the feedback circuit at all frequencies within the frequency range (col. 5, lines 12-55; right-hand side of Fig. 4; Fig. 6).

As for claim 31, Ferrero discloses (see the right-hand side of Fig. 4 ; Fig. 6; claim 1) an analyser for measuring the response of an electronic device to a high frequency input signal, the analyzer including:

an active load pull circuit connectable in use to a device to be analyzed (E), the active load pull circuit including

a feedback circuit (see the feedback circuit as shown in Fig. 4 and 6) arranged (i) to receive an output signal from the device to be analyzed (E), (ii) to modify the signal (using the band filter Rf, amplifier Am, and phase and magnitude control system represented by variable attenuator Ra and a variable phase shifter Rs), the modification including limiting the magnitude gain of the feedback circuit at frequencies (e.g. at frequencies from 500MHz to 19GHz) outside a band of frequencies (e.g., assumes that the band of frequencies is 20-110GHz, since applicant fails to specifically define the band of frequencies)and (iii) to feed the modified signal back to the device to be analyzed(E), the modified signal fed back comprising a component having a frequency within said band (e.g., 20-110GHz), and (iv) the feedback circuit is arranged to limit the magnitude gain of the feedback circuit at l frequencies inside the band of frequencies (e.g., 20-110GHz).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 23, 24, 28, 29, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferrero (U. S. Patent No. 6, 509,743).

As for claims 23 and 24, Ferrero discloses the method according to claim 16. Ferrero does not specifically disclose that the method is repeated and performed in respect of multiplicity of different modifications of the output signal from the device, or of the different input signals applied to the device. A person of ordinary skill in the art would find it obvious at the time of the invention to modify Ferrero to repeat and perform the method in respect of multiplicity of different modifications of the output signal as desired, or of the different input signals applied to the device, dependent upon the different applications on hands, for the purpose of analyzing the device with respect to different input/output conditions.

As for claims 28, 29, 32 and 33, Ferrero discloses the analyzer and a method of measuring according to claims 1 and 16 as discussed above. Ferrero does not specifically disclose a method of improving the design of a high frequency high power device or a method of manufacturing a high frequency high power device, including the steps of analyzing the behavior of the device by using the analyzer of claim 1 or performing the method of claim 16, and then modifying the design of the device in consideration of the results of the analyzing; and then manufacturing the device or the circuit in accordance with the improved design. A person of ordinary skill in the art would find it obvious at the time of the invention to modify Ferrero to disclose analyzing the behavior of the device by using the analyzer of claim 1 or performing the method of claim 16, and then modifying the design in consideration of the results, and then

manufacturing the device in accordance with the improved design, so as to make use of the analyzer device of Ferrero and improves on the device when needed.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferrero (U. S. Patent No. 6, 509,743) in view of Jeon et al. (U. S. Patent 7, 440,576).

As for claim 8, Ferrero discloses the analyser according to claim 1 as discussed above. Ferrero does not specifically disclose that the feedback circuit includes a heterodyne filter ring circuit.

Jeon et al. discloses using a conventional heterodyne filter ring circuit for frequency inversion and filtration and to improve the quality of the signal (abstract; Fig. 2; col. 3, line 31-col. 4, line 27).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Ferrero to incorporate the use of a heterodyne filter ring circuit in the feedback circuit, as taught by Jeon et al., for the purpose of filtering the high frequency signal with improved signal quality (abstract; Fig. 2; col. 3, line 31-col. 4, line 27).

Allowable Subject Matter

6. Claim 30 is allowed.

7. Claims 9, 11, 25, 26 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsironis (U. S. Pub No. 2004/020726) discloses an active load pull measurement system comprising two circulators, a band pass filter, a power amplifier, one variable attenuator, one stabilization tuner, a prematching tuner and a load tuner. The microwave stability of the set-up is improved by means of the band pass filter, which reduces the gain outside the frequency range of interest.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMY HE whose telephone number is (571)272-2230. The examiner can normally be reached on 9:30am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Amy He/
Examiner, Art Unit 2831